20 stripping away said organic photoresist layer;

applying a protective tape overlying said passivation layer and said passivation openings; and

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removing said protective tape wherein said gradually sloping sidewalls on said passivation openings allow said protective tape to be completely removed without leaving adhesive residue in the manufacture of the integrated circuit device.

## REMARKS

Examiner B. Kebede is thanked for the thorough examination and search of the subject Patent Application and for finding allowable subject matter in Claims 5, and 9 - 20. Claim 1 has been amended.

All Claims are believed to be in condition for Allowance, and that is so requested.

Reconsideration of Claims 1 - 4 and 6 - 8 rejected under 35 U.S.C. 103(a) as unpatentable over Applicant's Admitted Prior Art (AAPA) in view of Blalock (US 5,320,981) is requested based on Amended Claim 1 and on the following remarks.

Claim 1 has been amended such that a particular etching method is specified. In particular, Amended Claim 1 specifies:

. . .

reflowing said organic photoresist layer to create gradually sloping sidewalls on said organic photoresist layer;

thereafter etching through said passivation layer not covered by organic photoresist layer to form said passivation openings with gradually sloping sidewalls wherein said etching does not etch said organic photoresist layer;

. . .

The etching through step is amended such that (1) it follows the reflowing step and (2) it etches the passivation layer but not the photoresist layer. In this way, Amended Claim 1 specifies an method that is not taught nor suggested by Applicant's Admitted Prior Art, by Blalock, or by the combined teachings of Applicant's Admitted Prior Art in view of Blalock. In specific, the method of Blalock etches both the photoresist layer and the substrate at the same time.

Applicant respectfully believes that Amended Claim 1 should not be subject to rejection under 35 U.S.C. 103(a) as unpatentable over over Applicant's Admitted Prior Art (AAPA) in view of Blalock (US 5,320,981). In addition, Claims 2-4 and 6-8 represent patentably distinct further limitations on Amended Claim 1 and should also be in condition for allowance.

Reconsideration of Claims 1 - 4 and 6 - 8 rejected under 35 U.S.C. 103(a) as unpatentable over Applicant's Admitted Prior Art (AAPA) in view of Blalock (US 5,320,981) is requested based on Amended Claim 1 and on the above remarks.

Applicant has reviewed the prior art made of record and not relied upon and agrees with the Examiner that while the references are of general interest, they do not apply to the detailed Claims of the present invention.

Allowance of all Claims is requested.

Attached hereto is a marked-up version of the changes made to the Claims by the current amendment. The attached pages are captioned "VERSION WITH MARKINGS TO SHOW CHANGES MADE."

It is requested that should Examiner B. Kebede not find that the Claims are now Allowable that he call the undersigned at 989-686-3462 to overcome any problems preventing allowance.

Respectfully submitted,

Dougho R Schoolel

Douglas R. Schnabel, Reg. No. 47,927

## VERSION WITH MARKINGS TO SHOW CHANGES MADE

In the Claims:

Please Amend Claim 1 as follows:

1. (AMENDED) A method to form passivation openings that prevent protective tape residue in the manufacture of an integrated circuit device comprising:

providing a semiconductor substrate;

5 depositing a passivation layer overlying said semiconductor substrate;

depositing an organic photoresist layer overlying said passivation layer;

patterning said organic photoresist layer to expos

10 said passivation layer in areas where said passivation

openings are planned;

reflowing said organic photoresist layer to create gradually sloping sidewalls on said organic photoresist layer;

thereafter etching through said passivation layer not covered by organic photoresist layer to form said passivation openings with gradually sloping sidewalls

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wherein said etching does not etch said organic photoresist
layer;

stripping away said organic photoresist layer;

applying a protective tape overlying said passivation
layer and said passivation openings; and

removing said protective tape wherein said gradually sloping sidewalls on said passivation openings allow said protective tape to be completely removed without leaving adhesive residue in the manufacture of the integrated circuit device.